Extending Battery Life by Controlling Load Profile

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1. INTRODUCTION

Battery life can be extended by controlling how the load draws current from the battery. A "container of a fixed amount of energy" is a very poor model for real batteries. Informally, batteries follow the principle "What You Get Is How You Ask." A battery discharged at a high current compared to a low current not only drains faster as expected but also delivers less total energy into the load. This property originates in the chemical processes inside the battery that cannot be changed once the battery is manufactured. However, it is possible (albeit not always easy) to manipulate the current drawn by the load. This work investigates whether load current profile can be manipulate such that effective battery capacity is increased.

To extend battery life by load profile manipulations, two questions must be addressed:

- 1. Which load profile yields largest battery capacity?
- 2. How to isolate the load from the battery such that the current draw from the battery can be controlled without affecting the load?

This work focuses on the first question, but a brief discussion of the second challenge for a holistic view of the solution follows. The second question can be viewed as designing a mechanism for buffering energy. Such a mechanism can be a capacitor connected in parallel to the battery [?] or an capacitor whose charge is actively managed. An immediate difficulty with both approaches is the energy loss inherent in the charging process of the capacitor. It might be possible to use an LC charging circuit (plus a diode) for a charging process that is at least theoretically lossless [?]. A further difficulty with the former approach (capacitor in parallel with the battery) is unlimited charge current. Perhaps this could be addressed by adding current limiting circuitry between the battery and the capacitor, however the circuit used would need to not dissipate the excess as heat. In general, the buffering mechanism is not limited to capacitors. The energy that needs to be sourced from a hypothetical buffer may be provided by another power source such as an energy harvester from the environment or another battery.

The types of load targeted by this work are constant-current loads, not resistive loads. The load profiles generated are representative of loads that consume a constant amount of current in a given mode and can have multiple modes. Dig-

ital logic loads, such as a microcontroller or memory fall into this category. Resistive loads like a heating element do not and are not targeted by this work. An important load type that is left out by this category is digital logic powered through a linear voltage regulator. The current drawn by the digital logic is constant, but the current drawn by the voltage regulator depends on the input voltage. Maximizing the battery life under this kind of hybrid load is a separate question. Usually, increasing battery capacity, implies that its voltage will stay higher for a longer time. However, a higher voltage leads to more power dissipation in the regulator. Investigationg this problem of "more capacity implies more energy" falls outside the scope of the present work. This problem is avoided entirely by using highly-efficient switching regulators. In particular, designs that step up the voltage instead of stepping it down fundamentally avoid the need to dissipate excess power, which is at the root of the above problem.

2. BATTERY DISCHARGER

To explore how load current profile affects battery capacitor a battery discharger device was designed and built. The discharger fulfills three main objectives:

- 1. Generate a set of arbitrary load current profiles
- 2. Discharge a set of batteries according to each load profile
- 3. Collect a trace of battery voltage and (indirectly) load current

The discharge circuit must carry out the load profile despite variation in battery voltage and load resistance. A load profile specifies the desired discharge current at every discrete time step. The discharge circuit must maintain the specified discharge current through the load despite changes in battery voltage and variations in load resistance. The battery voltage varies because of (1) gradual discharging of the battery, and (2) voltage drop across the internal resistance of the battery. The load resistance may vary due to tempreture of the load resistor or variation in the component value. In order for these variations to not affect the discharge current the discharger is based on a current source.

The discharger must support concurrent experiments with different load profiles and multiple test batteries for each profile. Multi-way experiments are a first line of defense against hidden variables, such as environment temperature, since all batteries in one experiment are subject to the same conditions at every instant. Our prototyped device supports two load profiles with two batteries each. The approach scales to more load profiles and batteries at the cost of sampling rate, since ADC and IO hardware is multiplexed.

The next sub-sections describe the hardware and software that implement the above goals.

2.1 Hardware

The discharger architecture is shown in Figure 1. The TM4C123 (Tiva C) 32-bit microcontroller generates the load profile, acquires voltage data points, and sends the data to the host computer. Each battery is discharged by a voltagecontrolled transistor-based current source expanded in Figure 2. The current source sources current from the battery through a load resistor. Each current source is supplied by the battery voltage and controlled by an analog signal in the range of 0 to 3.3v. The resulting discharge current is approximately proportional to the magnitude of the analog signal (discussed further in Section 2.3 and Figure 5(b)). The microcontroller generates the digital load current values (see Section -2.2) which are converted to an analog voltage by a DAC. The DAC is implemented externally since TM4C123 microcontroller does not provide a built-in DAC peripheral. The DAC used in the prototype is a low-pass filter with an op-amp follower as shown in Figure 3. However, an improved design would use a dedicated DAC IC.

The device is capable of generating two load profiles concurrently and discharging two batteries per profile (see Section 2 for motivation). The two load profiles are referred to by letters (A, B), and the batteries within a profile by numbers (1, 2), which labels each battery under test as Xi, for example, Battery A1.

For each of the batteries, the voltage is sampled at the battery terminal (V_{bat}) and at the negative end of the load resistor $(V_c^{\ 1})$. The voltage at the base of the current source transistor (one per load profile) is also sampled for crosschecking and verification purposes. These samples are taken by one of the two ADCs in the TM4C microcontroller at a rate of 512 samples per second. Each voltage signal is sampled at this rate by multiplexing the ADC which has a raw sampling rate of 10⁶ samples per second. Each sample is an average of 16 back-to-back samples taken at the raw sampling rate of the ADC, which is computed in hardware. In addition, environment temperature is sampled once a second from the a sensor built into the microcontroller (mapped to a channel on the second ADC). All sampled data is transferred to the host computer via UART as described in more detail in Section 2.2.

The digital compare logic provided by the ADC module of the microcontroller is used to monitor the battery voltage and terminate the experiment once the voltage of *all* batteries has been observed below a specified threshold (1.8v). Analog comparators could be used for the same purpose, at the cost of somewhat more complex software to multiplex a

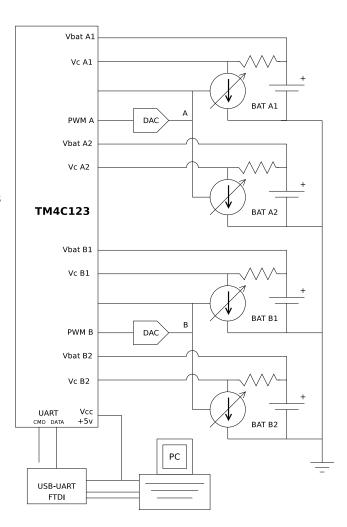


Figure 1: Battery discharger device (also see Figures 2 and 3)

limited number of them (two on TM4C123) or at the cost of extra external hardware. If battery voltage recovers after crossing the threshold, after the experiment has terminated, the experiment is not resumed. This models a load which will either shut off once the battery can no longer support it or cease to operate continuously correctly.

2.2 Software

The responsibilities of the software are

- 1. user command console
- 2. load profile generation
- 3. data acquisition and transfer to host
- stopping the experiment after all batteries have been drained

2.2.1 User command interface

The discharger device provides a text-driven console for taking commands from the user. Currently, the console supports commands for running a calibration routine and for

 $^{^1\}mathrm{In}~V_\mathrm{C}$ "C" stands for "collector" of the current source transistor.

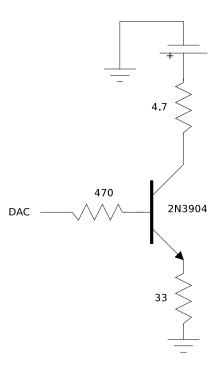


Figure 2: Voltage-controlled constant-current battery discharge circuit. Note: base resistors are shared by all current sources in one load profile.

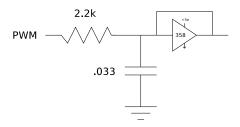


Figure 3: Digital-to-analog converter using a buffered low-pass filter

starting an experiment. Future extensions could include specifying load current profiles for the experiment (and committing them to non-volatile storage) and querying progress of the experiment (battery voltage). Initially, LEDs were flashed periodically as a heartbeat and upon transfer of buffer via UART. However, the current spikes due to turning on the LEDs propagated throughout the circuit and showed up in the acquired voltage traces. To address this, all LEDs were disabled except the crash LED that indicates an exception or assert failure. To verify that the experiment is running fine, the user can rely on the console or on the blinking LEDs on the FTDI board (separate in the prototype).

2.2.2 Load profile generation

Load profile is a step function of load current over time. All profiles are assumed to be periodic: the same sequence repeats over time. The user defines profile by specifying the step-function over one period as a set of intervals, each of which has a duration and a current magnitude. For example, to specify a constant current load of 50 mA, the profile would consist of one interval of any duration and a value of 50 mA. As another example, to specify a load that corresponds to an on/off waveform with a duty cycle of 25% and a period of 100 ms, two intervals would be given: (50 ms, 25 mA) and (50 ms, 0 mA). The loop that updates the output based on the specified step function runs at a period of 10ms. To be carried out exactly, the durations of the intervals need to be multiples of this period. The generator produces a PWM output with a duty cycle that matches the specified step-function. This PWM output is than converted to an analog voltage signal for controlling the discharger current source (see Section 2.1).

To be precise, in our prototype, to specify the current magnitude for each interval, the user actually specifies the duty cycle of the resulting PWM. This duty cycle is approximately proportional to the resulting current value (see Figure 5(b)) An improved version might take the input in mA and automatically convert it to the duty cycle by interpolating from the calibration data (Figure 5(b)) that is already obtained automatically by a calibration procedure. Note that calibration would still be necessary in an alternative design with a dedicated DAC since there is bound to be a discrepancy between the current-souce control signal and the resulting load current it sources from the battery.

2.2.3 Data acquisition

The voltage samples are transfered from the ADC by Direct-to-Memory (DMA) transfer. The DMA is configured to double-buffered mode so that samples are continuously transfered from the ADC without interruption for processing. Full buffers are transfered written to a UART port by another DMA routine. The buffers are transmitted as packets, which allows for flexibility in defining the sample streams. This is useful since different voltages may be sampled at different rates and be stored by different size buffers. The host-side Python tools assemble packets back into continuous streams.

2.2.4 Experiment termination

The experiment is over once all the batteries have been drained. This is detected by monitoring the battery volt-

ages and marking the batteries that have crossed a predefined threshold (1.8v) in a bitmask. Each time the bitmask is updated, it is checked whether all bits are set and if so, the experiment shutdown routine is run. Monitoring of battery voltage is implemented using digital comparator feature of the ADC module on TM4C: an ADC channel can be configured such that samples it acquires are automatically compared in hardware against a preset (digital) threshold and an interrupt is raised upon crossing of that threshold.

2.3 Calibration

The discharger circuit carries out the specified load profile by feeding an analog voltage control signal to the voltage-controlled current source that draws current from the battery. The control signal that is needed to generate a particular drain current needs to be estimated before the experiment. This procedure is referred to as *calibration*. To acquire the relationship between control signal and drain current, a special calibration load profile is carried out and voltage samples collected as usual. This load profile iterates over full control signal range in 10 discrete. ² The data is them automatically processed on a host tool to calculate the map between the control signal and the drain current. Battery drain current is the same as the current through the load resistor and is inferred from the voltage drop across the load resistor

$$I_{\mathrm{load}} = rac{V_{\mathrm{bat}} - V_{\mathrm{C}}}{R_{\mathrm{load}}}$$

Figure 4 shows an example of calibration trace from all batteries and Figure 5(a) shows processed trace and resulting control to load current map. The drain current is approximately proportional to the control voltage. However, this the relationship is not perfectly linear partially due to the voltage drop across base resistor.

Throughout all experiments environment temperature is collected by sampling a sensor built into the TM4C microcontroller. Figure 5 shows the temperature trace from Experiment 5. This data is not currently used for calibration or adjustment of data, however this might be done in the future.

3. EXPERIMENTAL METHODOLOGY

Batteries used in all experiments came from one of the two batches³ of Energizer CR2032VP (Japan, January 2012 and December 2012).

The resulting data from each experiment are the following quantities:

- Battery voltage, V_{bat} , for each battery: sampled from ADC at a fixed rate
- Collector voltage, $V_{\rm C}$, for each battery: sampled from ADC at a fixed rate

• Load current

$$I_{\text{load}} = \frac{V_{\text{bat}} - V_{\text{C}}}{R_{\text{load}}}$$

Battery capacity

$$C_{\text{bat}} = \int_0^T I_{\text{load}} dt$$

where T is the time when the voltage for the given battery has crossed the discharged threshold (2v in shown results).

• Internal resistance of the battery

$$R_{\mathrm{i}} = rac{V_{\mathrm{bat, unloaded}} - V_{\mathrm{bat}}}{I_{\mathrm{load}}}$$

where the unloaded battery voltage is measured by leaving the battery with a zero load current at the very beginning of each experiment.

• Rolling minimum battery voltage

$$V_{\mathrm{bat, min}}[i] = \min_{0 \le j \le i} V_{\mathrm{bat}}[j]$$

where indices i and j denote samples. The rolling minimum voltage illustrates the discharging of the battery in a way that raw V_{bat} cannot since the latter recovers whenever the load load current is zero.

3.1 Despiking: outlier correction

The voltage trace data was found to contain outliers in the form of spikes as shown in Figure 7. These spikes go in either positive or negative direction. Only one data point is affected, not several consecutive points. The working hypothesis for the source of these spikes is electrical interference in the circuit that affects the ADC readings. A host-side tool was written to detect these spikes by looking for three data points in the shape of a spike (without matching sudden but persistent transitions). Each spike was replaced by a value interpolated from the two points at the base of the spike.

4. RESULTS

The following three experiments were performed ⁴

- 1. effect of discharge rate on capacity
- 2. effect of peak current on capacity
- 3. effect of period on capacity (in duty-cycled loads)

The discharge rate experiment subjects the battery to a constant discharge current. The peak current experiment fixes an average current draw to 25mA and considers three different load profiles that achieve that same average current. In the period experiment, the load profiles are on/off waveforms of a fixed duty cycle (50%) and a fixed on-current (50mA) but a different period.

Each experiment was performed with two different profiles being applied to two batteries each concurrently. Concurrent runs control for hidden variables by having all batteries subjected to the same conditions. However, the results

 $^{^2{\}rm Since}$ in our prototype the profile waveform is specified in terms of the PWM duty cycle (Section 2.2.2), the iteration is over duty cycle values.

³Batteries in one experiment are from the same batch.

⁴The experiment numbers in the figures do not match the numbers in this list.

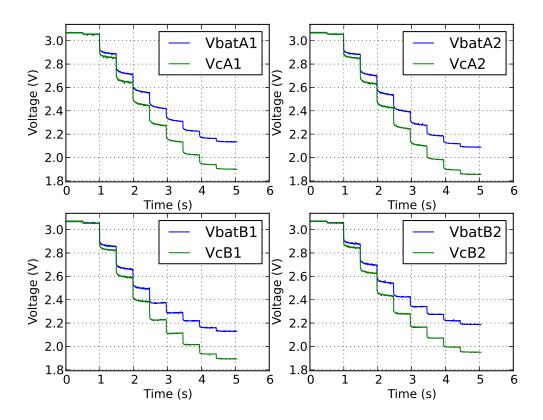
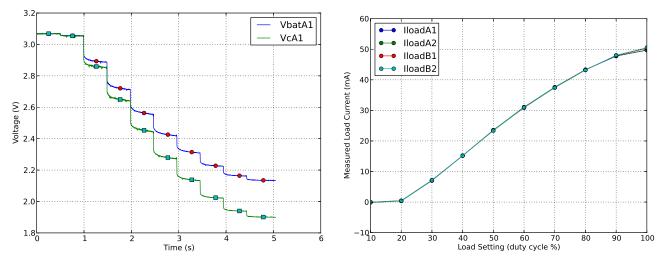


Figure 4: Battery and collector voltage trace for a sequence of load currents used for calibration.



(a) Battery and collector voltage trace for battery A1 with (b) Measured load current as a function of the control setting detected load current levels marked

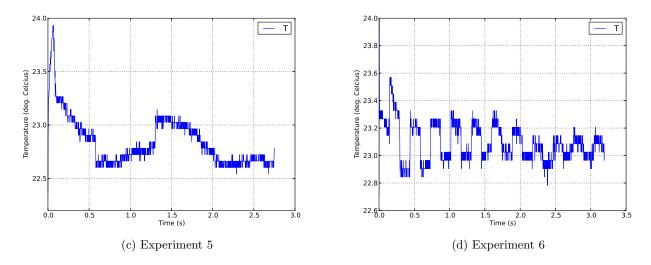


Figure 5: Temperature during experiment runs measured by the internal sensor in the microcontroller.

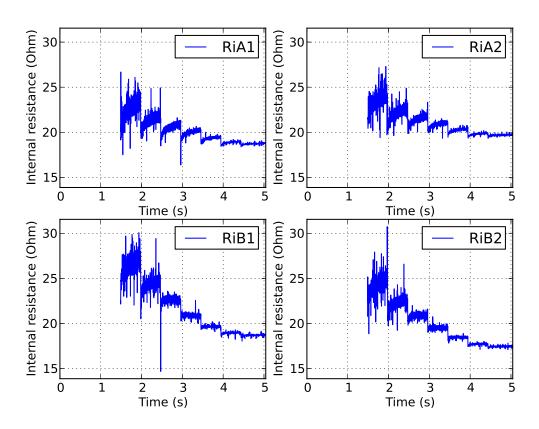


Figure 6: Internal resitance (R_i) for the calibration trace.

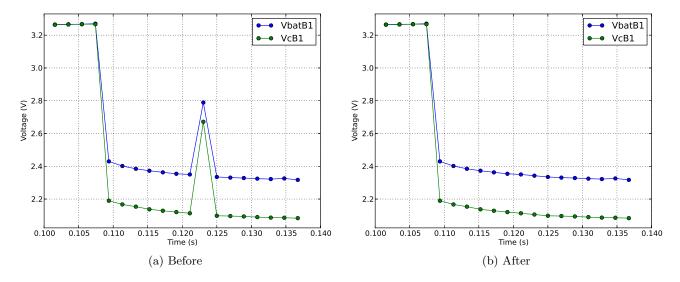


Figure 7: "Despiking" operation applied to an example trace to remove erroneous data points due to electrical interference in the circuit.

shown include data from sequential runs of the experiments in order to increase the number of data points.

All experiments were performed with discharge currents on the order of 20-50mA, in order to shorten the duration of the experiments. The employed drain current is two-orders of magnitude larger than the current of 0.2 mA at which the battery capacity specified in the datasheet (240 mAh) was rated. The battery capacity at the employed drain currents is two-orders of magnitude smaller than the rated capacity and is on the order of 5mAh. To strengthen the study, further experiments at more typical discharge currents need to be performed.

Figures 8, 9, 10 show how battery capacity is affected by each of the three studied factors. The effect of the discharge rate is the most pronounced (and most well known). The lower the peak current, the higher the effective battery capacity. This effect is more pronounced at lower drain currents. There is insufficient data to draw conclusions about the affect of period on battery capacity, however the observation that is *not* statistically significant that can be drawn from the data is that longer periods are detrimental to effective battery capacity.

5. CONCLUSION AND FUTURE WORK

This work has explored how battery capacity is affected by the load current with the ultimate goal of manipulating the latter to extend battery life. A tangible outcome of this work is a working prototype device for discharging batteries according to arbitrary specifiable load current profiles. The discharger device was used to run three experiments to study three different aspects of the load profile that affect effective battery capacity: average drain current, peak current, and period (in duty cycled loads). We have found that each of these has an measurable effect. Factors that have a decrease the effective battery capacity are high drain current, high peak current (for the same average current), and long period (in duty cycled loads).

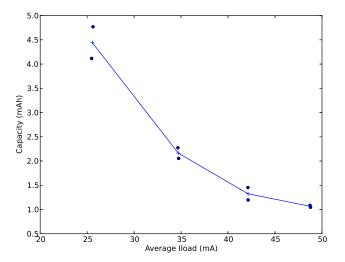


Figure 8: Battery capacity as a function of continuous drain current. Points marked by circles are from Experiments 2 and 4, crosses are averages of those points.

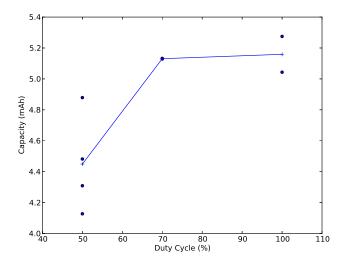


Figure 9: Battery capacity as a function of load profiles with the same average power but varying duty cycles (current in active part of the cycle inversely proportional to duty cycle). Points marked by circles are from Experiments 1 and 5, crosses are averages of those points.

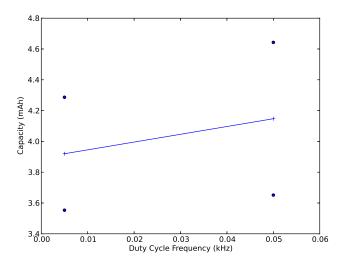


Figure 10: Battery capacity as a function of load profiles with the same average power but varying duty cycles (current in active part of the cycle inversely proportional to duty cycle). Points marked by circles are from Experiments 1 and 5, crosses are averages of those points.

Future work involves committing the discharger device to a PCB, which requires some design refinements, and scaling it to more batteries (by a factor of about four). Scaling of the device might involve moving the current integration to compute the battery capacity on-board to reduce the I/O bandwidth demand. The experiments need to be repeated with many more data points (batteries) for for each profile as well as for more profile variations ("x-axis values"). A wider range of time scales needs to be explored to capture battery behavior that is due to chemical processes that take place only at those timescales. The experiments should be conducted in a temperature-controlled environment to minimize the significant variation in battery capacity caused by temperature changes. Finally, the complimentary research question of how to buffer energy transparently to the load remains open.

APPENDIX

A. MEASURED AND COMPUTED QUAN-TITIES FROM ALL EXPERIMENTS

For each experiment, we present the trace of battery voltage and collector voltage, rolling minimum battery voltage, load current, and battery internal resistance (see Section 3 for definitions).

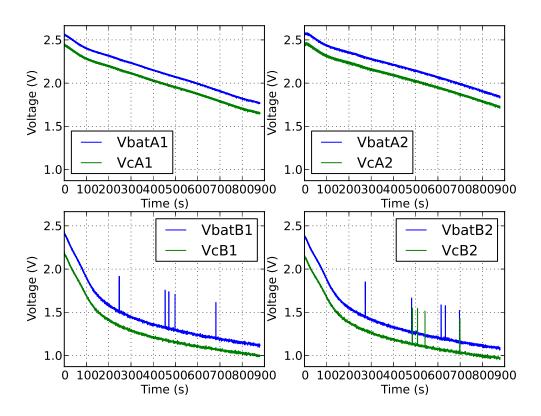


Figure 11: Experiment 2 (continuous drain A=25mA (52% d.c.) and B=50mA (92% d.c.)): battery and collector voltage trace.

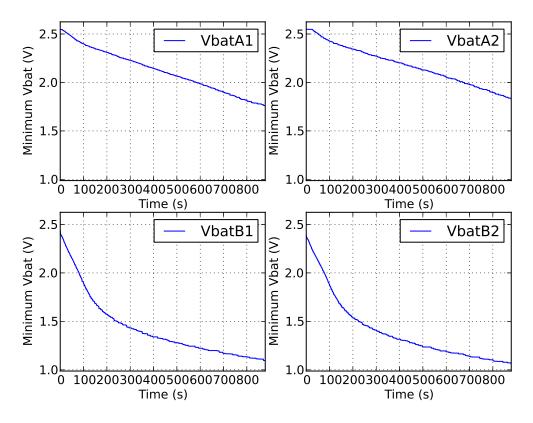


Figure 12: Experiment 2 (continuous drain A=25mA (52% d.c.) and B=50mA (92% d.c.)): rolling minimum battery voltage.

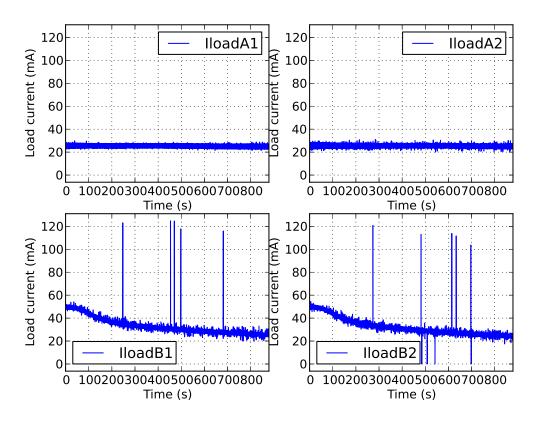


Figure 13: Experiment 2 (continuous drain A = 25mA (52% d.c.) and B = 50mA (92% d.c.)): load current.

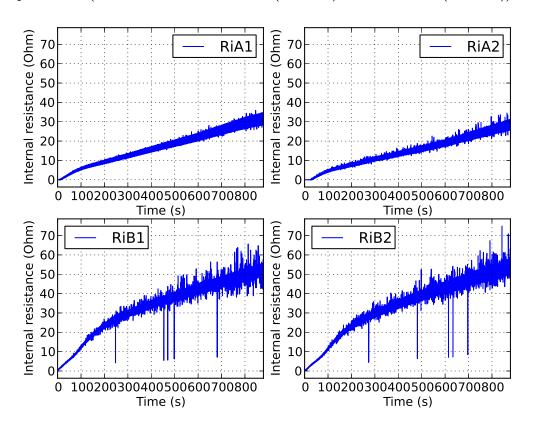


Figure 14: Experiment 2 (continuous drain A=25mA (52% d.c.) and B=50mA (92% d.c.)): internal resistance.

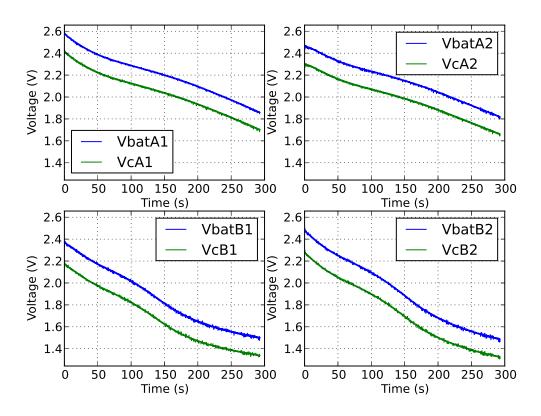


Figure 15: Experiment 4 (continuous drain A=35mA (65% d.c.) and B=42mA (78% d.c.)): battery and collector voltage trace.

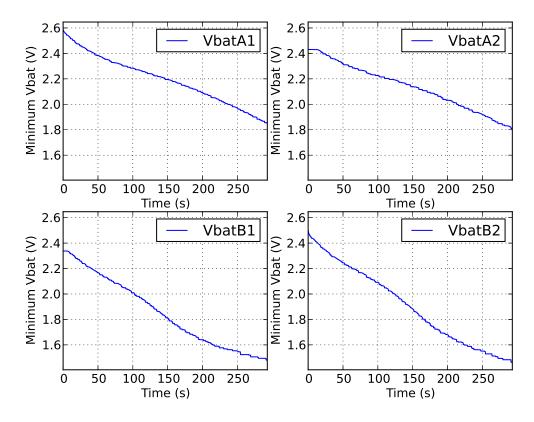


Figure 16: Experiment 4 (continuous drain A=35mA (65% d.c.) and B=42mA (78% d.c.)): rolling minimum battery voltage.

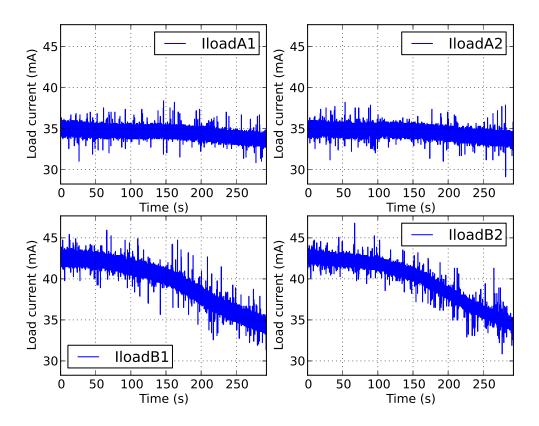


Figure 17: Experiment 4 (continuous drain A=35mA (65% d.c.) and B=42mA (78% d.c.)): load current.

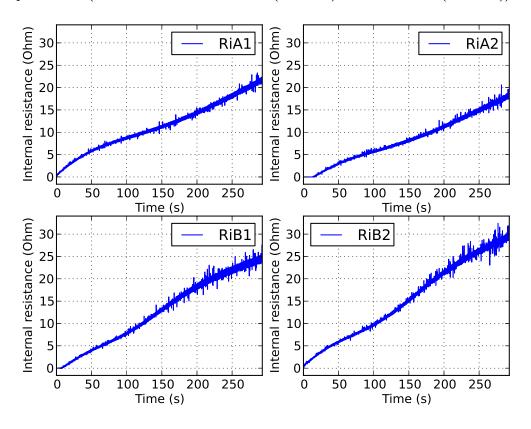


Figure 18: Experiment 4 (continuous drain A=35mA (65% d.c.) and B=42mA (78% d.c.)): internal resistance.

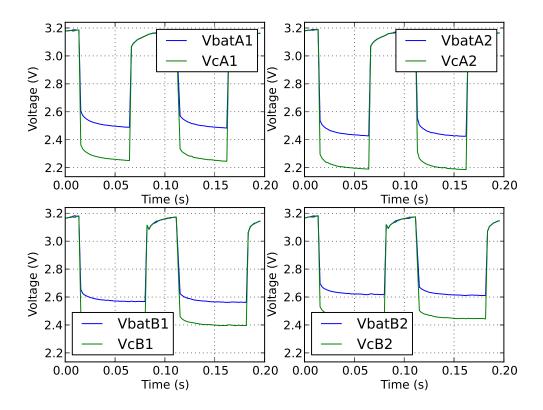


Figure 19: Experiment 5 (A = 50% d.c. of 50mA (95% load d.c.) and B = 70% d.c. of 36mA (66% load d.c.)): battery and collector voltage trace over a short initial interval to show detail.

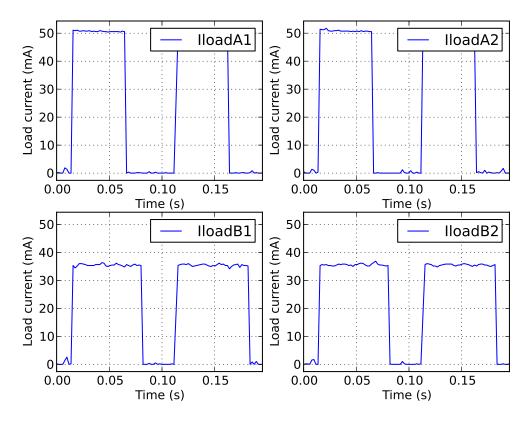


Figure 20: Experiment 5 (A = 50% d.c. of 50mA (95% load d.c.) and B = 70% d.c. of 36mA (66% load d.c.)): load current over a short initial interval to show detail.

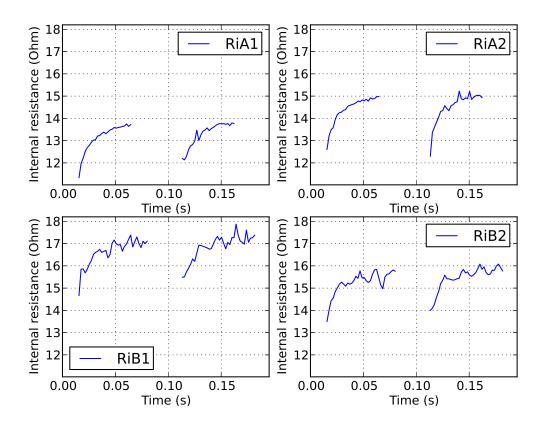


Figure 21: Experiment 5 (A = 50% d.c. of 50mA (95% load d.c.) and B = 70% d.c. of 36mA (66% load d.c.)): internal resistance over a short initial interval to show detail.

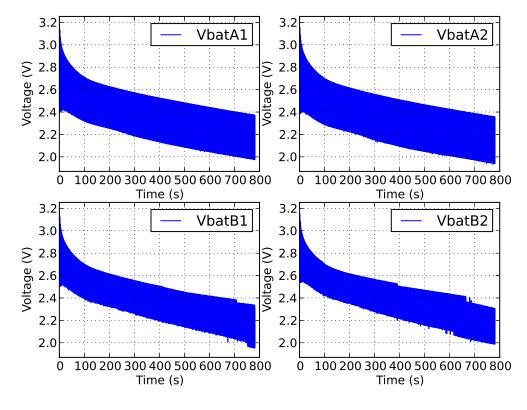


Figure 22: Experiment 5 (A = 50% d.c. of 50mA (95% load d.c.) and B = 70% d.c. of 36mA (66% load d.c.)): battery and collector voltage trace.

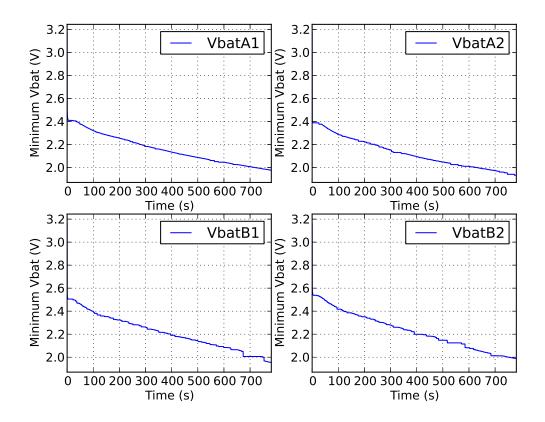


Figure 23: Experiment 5 (A = 50% d.c. of 50mA (95% load d.c.) and B = 70% d.c. of 36mA (66% load d.c.)): rolling minimum battery voltage.

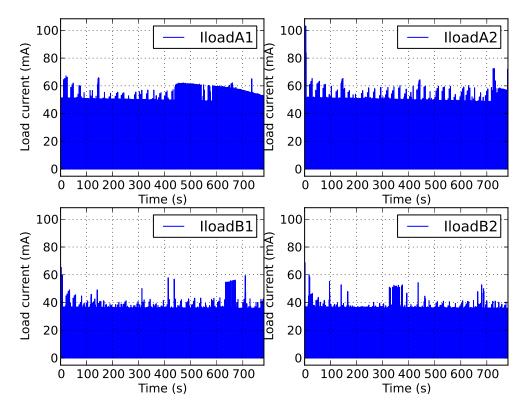


Figure 24: Experiment 5 (A = 50% d.c. of 50mA (95% load d.c.) and B = 70% d.c. of 36mA (66% load d.c.)): load current.

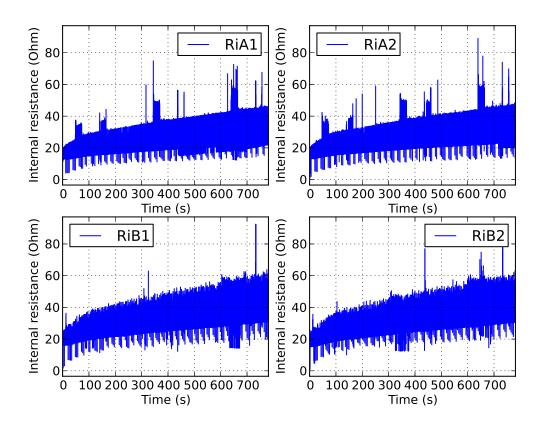


Figure 25: Experiment 5 (A = 50% d.c. of 50mA (95% load d.c.) and B = 70% d.c. of 36mA (66% load d.c.)): internal resistance.

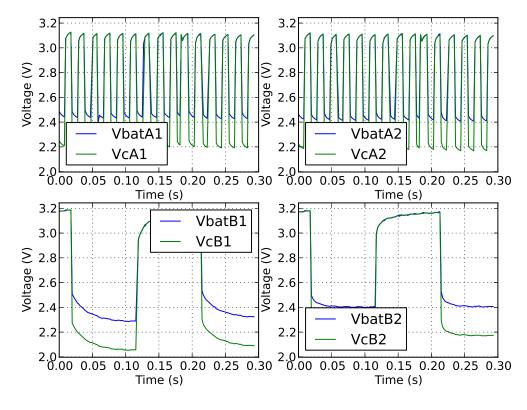


Figure 26: Experiment 6 (at 50mA (92% d.c.) A = 10ms every 20ms and B = 100ms every 200ms): battery and collector voltage trace over a short initial interval to show detail.

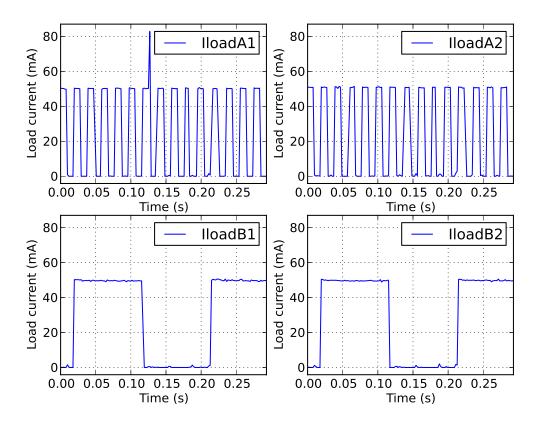


Figure 27: Experiment 6 (at 50mA (92% d.c.) A = 10ms every 20ms and B = 100ms every 200ms): load current over a short initial interval to show detail.

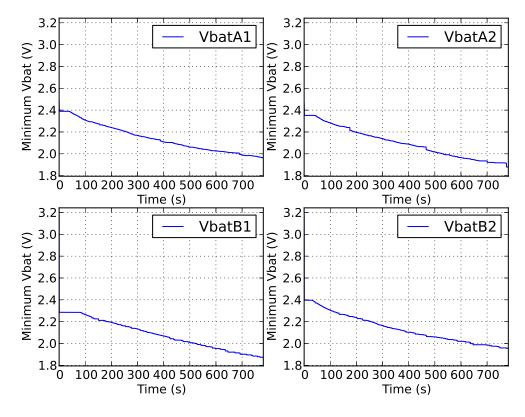


Figure 28: Experiment 6 (at 50mA (92% d.c.) A=10ms every 20ms and B=100ms every 200ms): rolling minimum battery voltage.

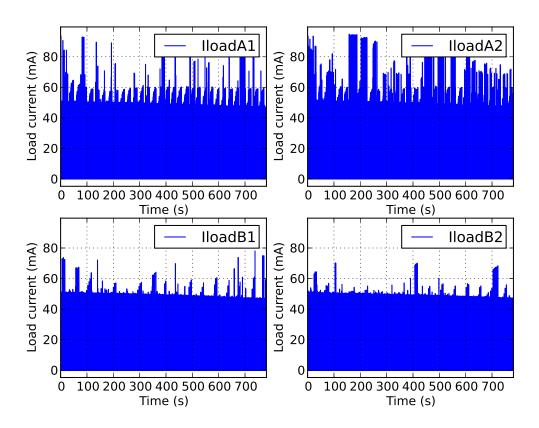


Figure 29: Experiment 6 (at 50mA (92% d.c.) A = 10ms every 20ms and B = 100ms every 200ms): load current.

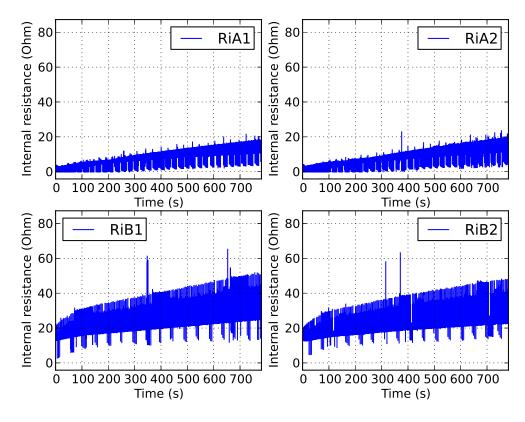


Figure 30: Experiment 6 (at 50mA (92% d.c.) A = 10ms every 20ms and B = 100ms every 200ms): internal resistance.